FIG. 1

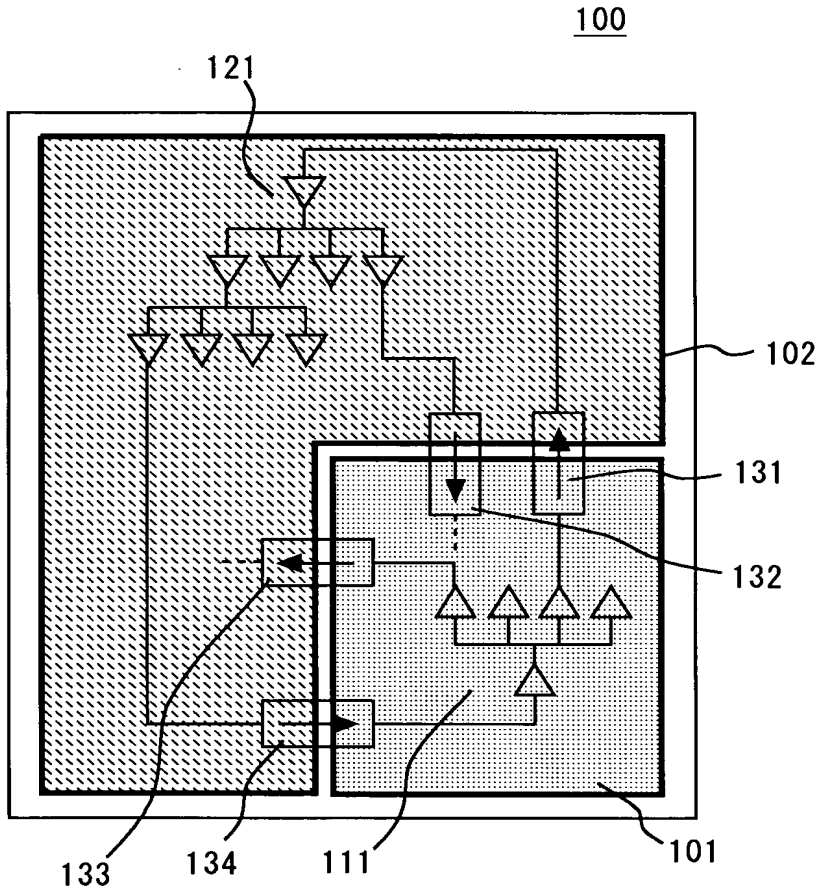


FIG. 2A

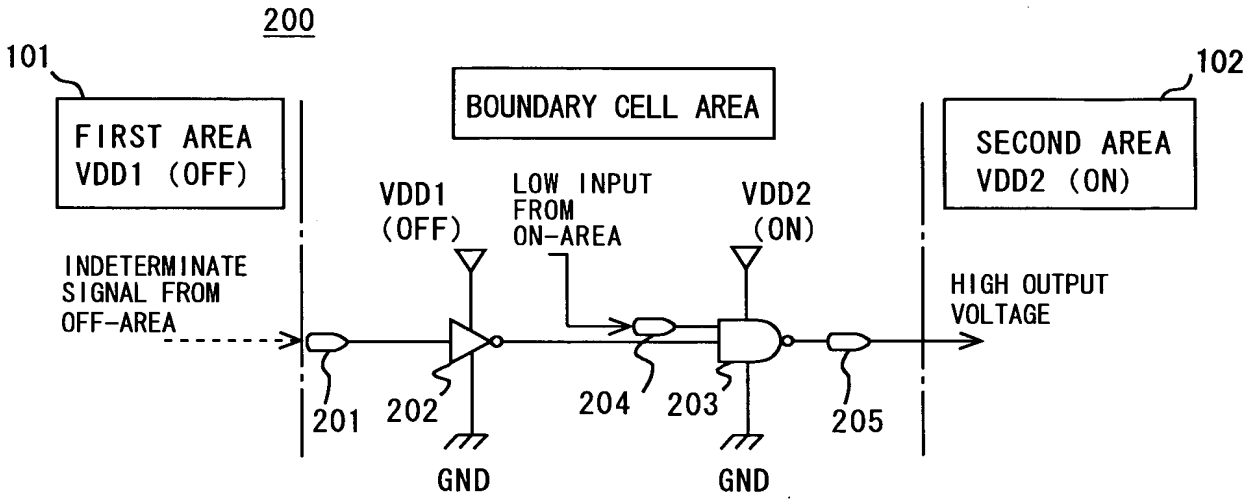


FIG. 2B

INPUT	ENABLE	OUTPUT
0	1	0
1	1	1
X	1	X
X	0	1
X	X	X

FIG. 3A

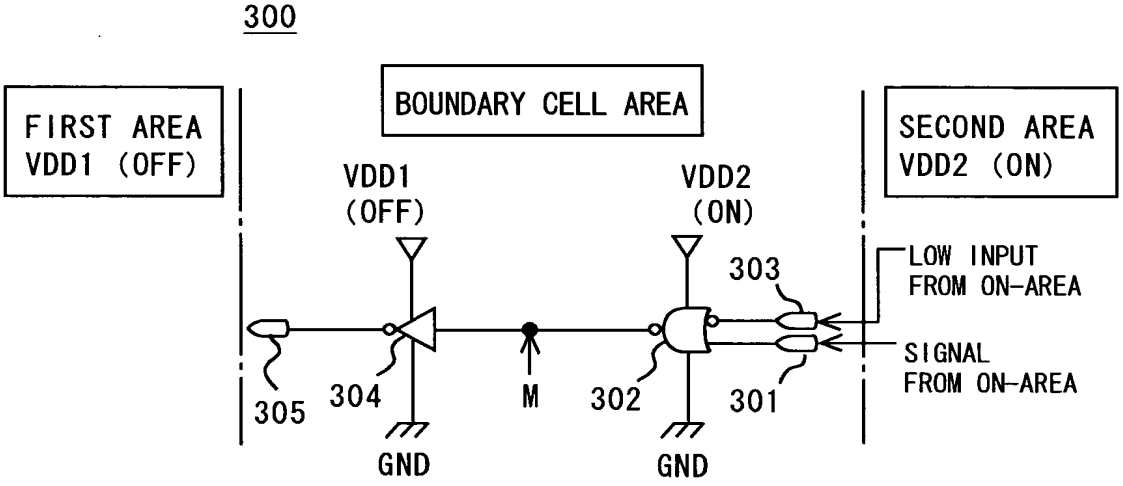


FIG. 3B

INPUT	ENABLE	M	OUTPUT
0	1	1	0
1	1	0	1
X	1	X	X
X	0	0	1
X	X	X	X

FIG. 4A

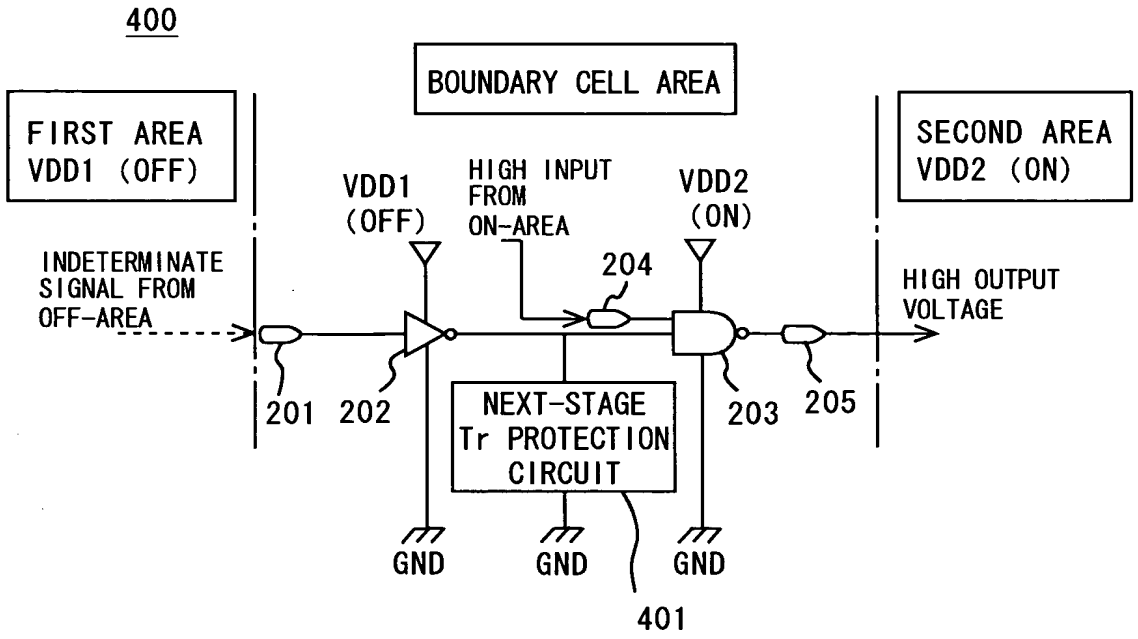


FIG. 4B

INPUT	ENABLE	OUTPUT
0	1	0
1	1	1
X	1	X
X	0	1
X	X	X

FIG. 5A

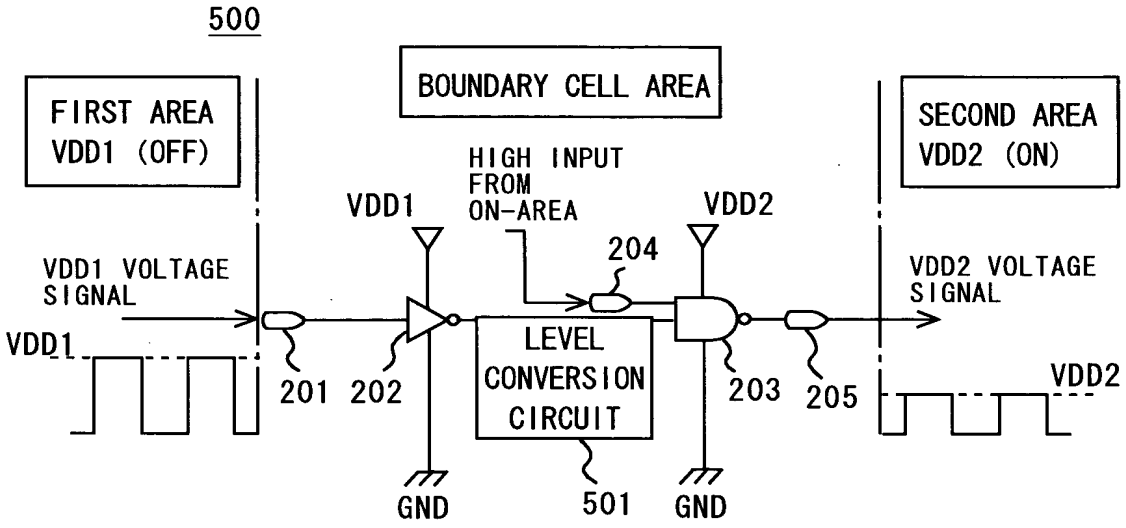


FIG. 5B

INPUT	ENABLE	OUTPUT
0	1	0
1	1	1
X	1	X
X	0	1
X	X	X

FIG. 6

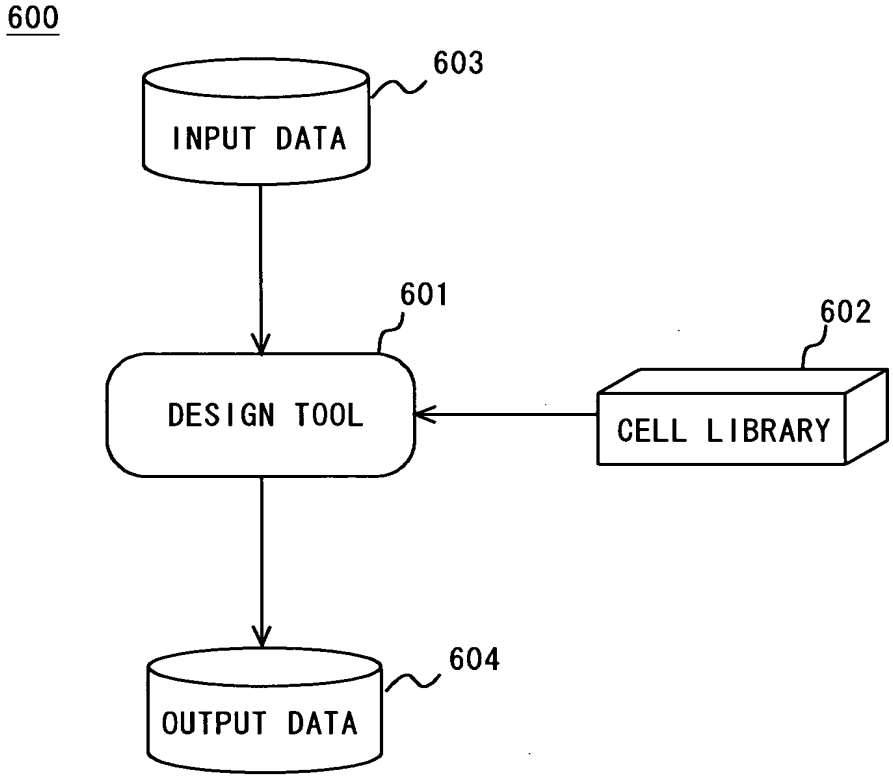

600
603
INPUT DATA
601
602
DESIGN TOOL
CELL LIBRARY
604
OUTPUT DATA

FIG. 7

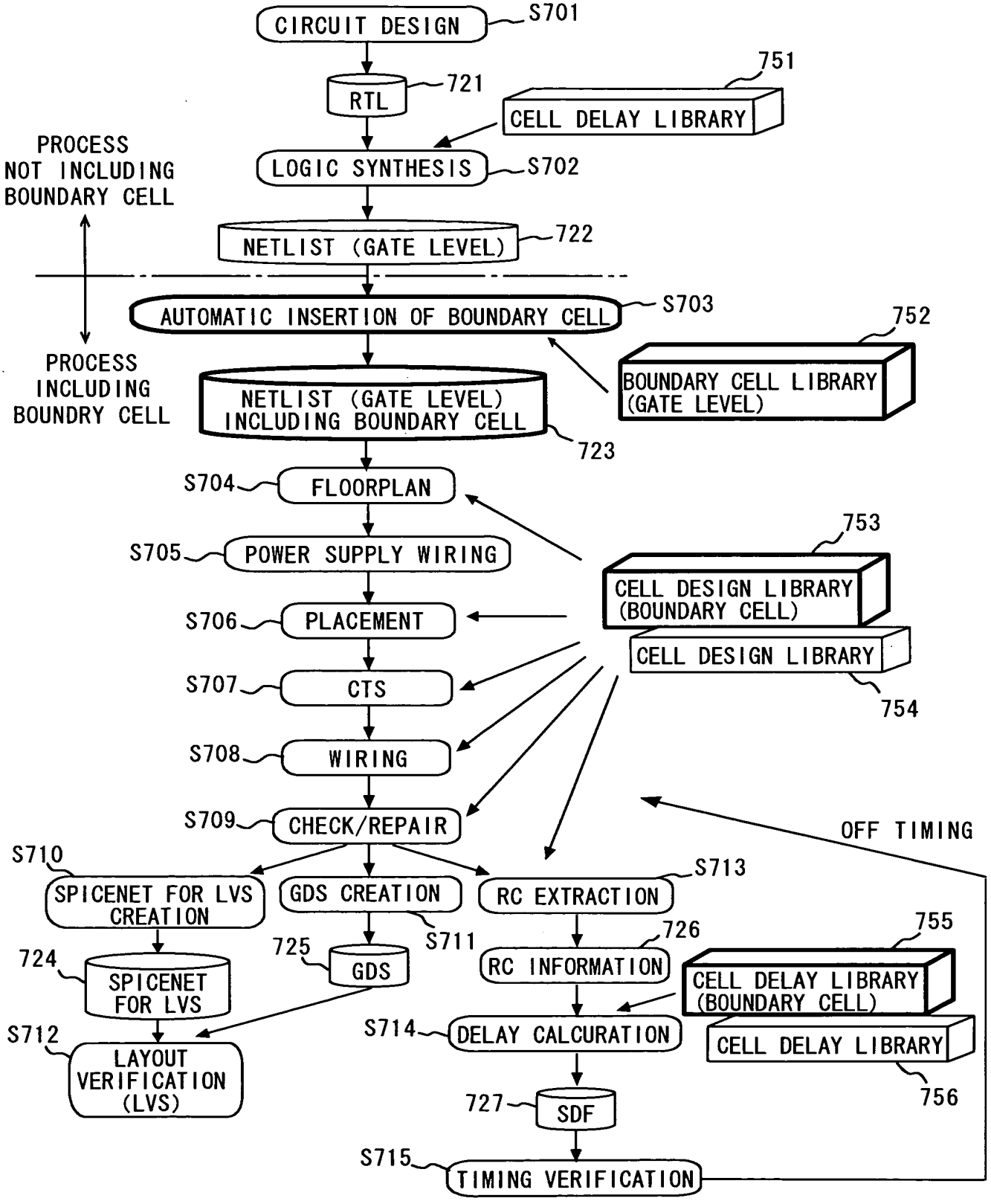
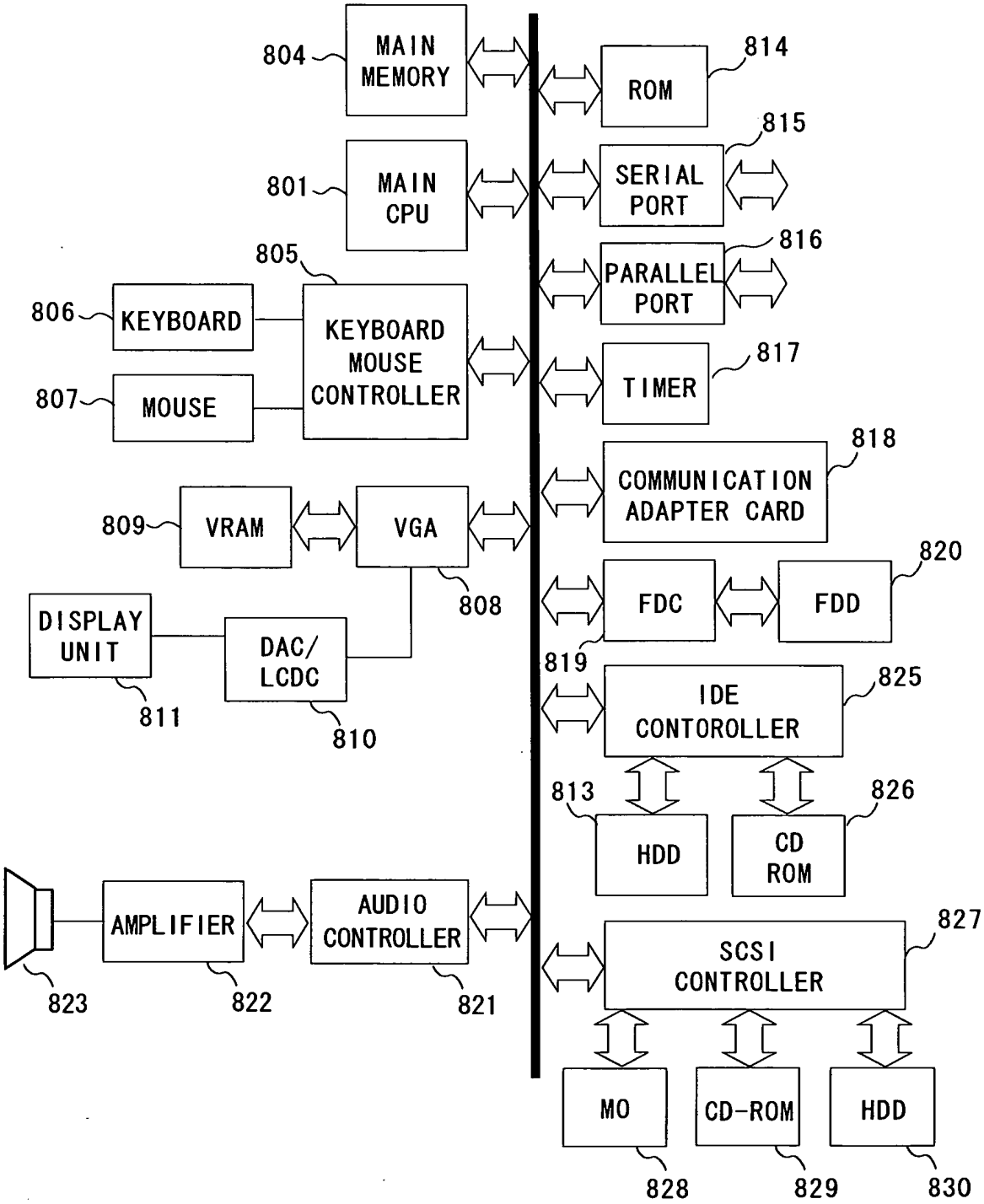

CIRCUIT DESIGN
S701
RTL
721
751
CELL DELAY LIBRARY
PROCESS NOT INCLUDING BOUNDARY CELL
LOGIC SYNTHESIS
S702
NETLIST (GATE LEVEL)
722
AUTOMATIC INSERTION OF BOUNDARY CELL
S703
752
BOUNDARY CELL LIBRARY (GATE LEVEL)
PROCESS INCLUDING BOUNDRY CELL
NETLIST (GATE LEVEL) INCLUDING BOUNDARY CELL
723
S704
FLOORPLAN
753
S705
POWER SUPPLY WIRING
CELL DESIGN LIBRARY (BOUNDARY CELL)
S706
PLACEMENT
CELL DESIGN LIBRARY
754
S707
CTS
S708
WIRING
S709
CHECK/REPAIR
OFF TIMING
S710
SPICENET FOR LVS CREATION
GDS CREATION
S711
S713
RC EXTRACTION
724
SPICENET FOR LVS
725
GDS
726
RC INFORMATION
755
CELL DELAY LIBRARY (BOUNDARY CELL)
S712
LAYOUT VERIFICATION (LVS)
S714
DELAY CALCURATION
CELL DELAY LIBRARY
756
727
SDF
S715
TIMING VERIFICATION

FIG. 8


804
MAIN MEMORY
814
ROM
815
801
MAIN CPU
SERIAL PORT
816
805
PARALLEL PORT
806
KEYBOARD
KEYBOARD MOUSE CONTROLLER
817
807
MOUSE
TIMER
818
COMMUNICATION ADAPTER CARD
809
VRAM
VGA
820
808
FDC
FDD
DISPLAY UNIT
DAC/ LCDC
819
825
IDE CONTOROLLER
811
810
813
826
HDD
CD ROM
827
AMPLIFIER
AUDIO CONTROLLER
SCSI CONTROLLER
823
822
821
MO
CD-ROM
HDD
828
829
830